

What is claimed is:

1. A method of designing a circuit layout of a semiconductor integrated circuit, comprising:

designing a logic function of the integrated circuit;

5 designing a pattern layout of the integrated circuit so that the pattern layout includes a logic cell area and an open area;

inserting a spare underground cell into the open area, wherein the spare underground cell includes a functional element;

10 and

designing a mask layout of the integrated circuit, the mask layout including the logic cell and the spare underground cell.

2. A method of designing a circuit layout according to claim 1, wherein the functional element includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit, an exclusive OR circuit and a latch circuit.

3. A method of designing a circuit layout according to claim 1, wherein inserting the spare underground cell includes:

20 dividing the pattern layout into a plurality of block regions;

searching the open area from the block regions;

distributing the open area into the block regions; and

inserting the spare underground cell into the distributed

25 open area.

4. A method of designing a circuit layout according to claim 3, wherein the inserting the spare underground cell into the distributed open area includes:

pointing out an open area in an attended block region and
5 an attended spare underground cell;

inserting the attended spare underground cell into the open area in the attended block region;

renewing the attended block region; and

setting a flag when all inserting within the attended block
10 region are finished.

5. A method of designing a circuit layout according to claim 4, wherein the inserting the spare underground cell into the distributed open area further includes:

renewing the attended spare underground cell; and

15 repeating the pointing out, the inserting the attended spare underground cell, renewing the attended block region, setting and renewing the attended spare underground cell with another open area in another attended block region and another attended spare underground cell until all of the block regions
20 are finished.

6. A method of changing a circuit layout of a semiconductor integrated circuit, comprising:

preparing the circuit layout including a logic cell area and a spare underground cell area, wherein the spare underground
25 cell area includes a functional element;

hypothetically disposing a changing layout into the spare underground cell area;

preparing a list of the changing layout;

deciding the position of the changing layout; and

5 automatically setting a conductive pattern layout of the semiconductor integrated circuit.

7. A method of changing a circuit layout according to claim 6, wherein the functional element includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit an exclusive OR circuit
10 and a latch circuit.

8. A method of changing a circuit layout according to claim 6, wherein the disposing includes:

deleting a logic cell to be changed; and

adding a spare underground cell for replacing the deleted
15 logic cell in the spare underground cell area.

9. A method of changing a circuit layout according to claim 6, further comprising designing a mask of the semiconductor integrated circuit after the setting.

10. A method of designing a circuit layout of a
20 semiconductor integrated circuit, comprising:

designing a logic function of the integrated circuit;

designing a pattern layout of the integrated circuit so as to include a plurality of logic cells in a logic cell area and an open area;

25 inserting a plurality of spare underground cells into the

open area, wherein each of the spare underground cells includes a plurality of functional elements; and

designing a mask layout of the integrated circuit, the mask layout including the logic cells and the spare underground
5 cells.

11. A method of designing a circuit layout according to claim 10, wherein the functional elements includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit an exclusive OR circuit and a latch circuit.

10 12. A method of designing a circuit layout according to claim 10, wherein each of the spare underground cells has a same kind of the functional elements.

13. A method of designing a circuit layout according to claim 10, wherein inserting the spare underground cells includes:

15 dividing the pattern layout into a plurality of block regions;

searching the open area from the block regions;

distributing the open area into the block regions; and

inserting the spare underground cells into the distributed

20 open area.

14. A method of designing a circuit layout according to claim 13, wherein the inserting the spare underground cells into the distributed open area includes:

pointing out an open area in an attended block region and
25 an attended spare underground cell;

inserting the attended spare underground cell into the open area in the attended block region;

renewing the attended block region; and

setting a flag when all inserting within the attended block region are finished.

15. A method of designing a circuit layout according to claim 14, wherein the inserting the spare underground cells into the distributed open area further includes:

renewing the attended spare underground cell; and

10 repeating the pointing out, the inserting the attended spare underground cell, renewing the attended block region, setting and renewing the attended spare underground cell with another open area in another attended block region and another attended spare underground cell until all of the block regions
15 are finished.